Trials@uspto.gov
571-272-7822

Paper No. 10
Date: January 26, 2022

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

PATENT QUALITY ASSURANCE, LLC,
Petitioner,

v.

VLSI TECHNOLOGY LLC,
Patent Owner.

IPR2021-01229
Patent 7,523,373 B2

Before THOMAS L. GIANNETTI, BRIAN J. MCNAMARA, and JASON W. MELVIN, *Administrative Patent Judges*.

MELVIN, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Patent Quality Assurance, LLC ("Petitioner") filed a Petition (Paper 1, "Pet.") requesting institution of *inter partes* review of claims 1–16 (all claims, or "the challenged claims") of U.S. Patent No. 7,523,373 B2 (Ex. 1001, "the '373 patent"). VLSI Technology LLC ("Patent Owner") filed a Preliminary Response. Paper 7 ("Prelim. Resp."). As authorized, Petitioner filed a Preliminary Reply (Paper 8 ("Prelim. Reply")), and Patent Owner filed a Preliminary Sur-Reply (Paper 9("Prelim. Sur-Reply")).

An *inter partes* review may not be instituted unless "the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a). For the reasons set forth below, we conclude that Petitioner has shown a reasonable likelihood it will prevail in establishing the unpatentability of at least one challenged claim, and we institute *inter partes* review.

A. RELATED MATTERS

The parties both identify the following matters related to the '373 patent: *VLSI Technology LLC v. Intel Corporation*, No. 1:19-cv-00254-ADA (consolidated as 1:19-cv-00977) (W.D. Tex.) (trial concluded with jury verdict); and *OpenSky Industries, LLC v. VLSI Tech. LLC*, IPR2021-01056. Pet. 75; Paper 4.

Patent Owner identifies the following additional matters: *VLSI Tech. LLC v. Intel Corp.*, No. 6:21-cv-00057 (W.D. Tex.); *VLSI Tech. LLC v. Intel Corp.*, No. 6:21-cv-00299 (W.D. Tex.); and *Intel Corp. v. VLSI Tech. LLC*, IPR2020-00158 (PTAB) (on appeal to Federal Circuit, No. 21-1616). Paper 4.

B. REAL PARTIES IN INTEREST

Petitioner identifies only itself as the real party in interest. Pet. 75. Patent Owner identifies VLSI Technology LLC and CF VLSI Holdings LLC as real parties in interest. Paper 4.

C. THE '373 PATENT

The '373 patent is titled Minimum Memory Operating Voltage Technique. Ex. 1001, code (54). It describes a method of determining the minimum operating voltage for integrated-circuit memory, storing the value of that voltage in nonvolatile memory, and using the value to determine when an alternative power-supply voltage may be switched to the memory or ensuring that the minimum operating voltage is otherwise met. *Id.*, code (57).

The '373 patent's Figure 1 is reproduced below:

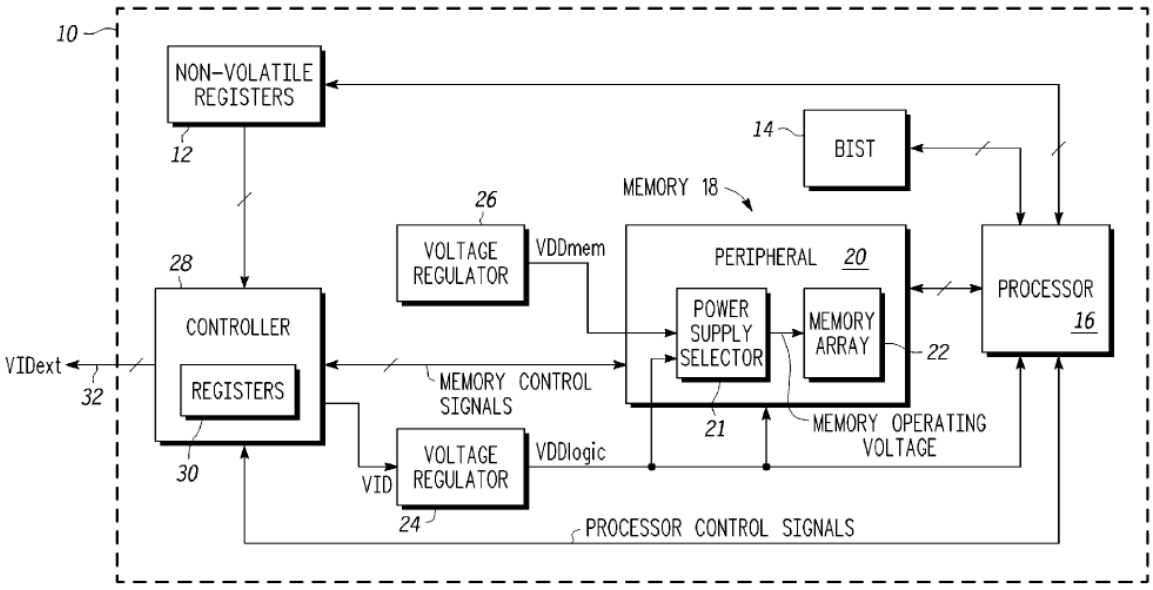

FIG. 1

Ex. 1001, Fig. 1. Figure 1 depicts data processing system 10 including processor 16, voltage regulators 24 and 26, and memory 18 that includes power supply selector 21. *Id.* at 2:38–57. Power supply selector 21 "selects one of VDDmem and VDDlogic and provides one of these to memory array 22 as the memory operating voltage." *Id.* at 2:52–55.

D. Challenged Claims

Challenged claim 1 is reproduced below:

1. A method, comprising:

[a] providing an integrated circuit with a memory;

[b] operating the memory with an operating voltage;

[c] determining a value of a minimum operating voltage of the memory;

[d.1] providing a non-volatile memory (NVM) location;

[d.2] storing the value of the minimum operating voltage of the memory in the NVM location;

[1e] providing a functional circuit on the integrated circuit exclusive of the memory;

[1f] providing a first regulated voltage to the functional circuit;

[1g] providing a second regulated voltage, the second regulated voltage is greater than the first regulated voltage;

[1h] providing the first regulated voltage as the operating voltage of the memory when the first regulated voltage is at least the value of the minimum operating voltage; and

[i] providing the second regulated voltage as the operating voltage of the memory when the first regulated voltage is less than the value of the minimum operating voltage, [j] wherein while the second regulated voltage is provided as the operating voltage of the memory, the

first regulated voltage is provided to the functional circuit.

Ex. 1001, 13:7–28.[1] Claims 9 and 16 are independent and recite limitations similar to claim 1. *Id.* at 13:59–14:15, 14:40–62. Claims 2–8 each depend from claim 1; claims 10–15 depend, directly or indirectly, from claim 9. *Id.* at 13:29–14:39.

E. PRIOR ART AND ASSERTED GROUNDS

Petitioner asserts the following grounds of unpatentability:

Claim(s) Challenged	35 U.S.C. §	References/Basis
1–7, 9–11, 13–16	103	Harris,[2] Abadeer,[3] Zhang[4]
2, 11, 12	103	Harris, Abadeer, Zhang, Cornwell[5]
8	103	Harris, Abadeer, Zhang, Bilak[6]

Pet. 2. Petitioner relies also on the Declaration of Adit Singh, Ph.D. (Ex. 1002) and the Declaration of Sylvia D. Hall-Ellis, Ph.D. (Ex. 1027).

II. ANALYSIS

A. DISCRETIONARY DENIAL

1. District-court litigation

Patent Owner argues that we should deny institution under *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (Mar. 20, 2020) (precedential).

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[1] Our bracketed designations for limitations largely follow those used by the parties. *See* Pet. 25–46.
[2] US 5,867,719, issued Feb. 2, 1999 (Ex. 1003).
[3] US Pub. 2006/0259840 A1, published Nov. 16, 2006 (Ex. 1004).
[4] US Pub. 2003/0122429 A1, published July 3, 2003 (Ex. 1005).
[5] US 7,702,935 B2, issued Apr. 20, 2010 (Ex. 1006).
[6] US Pub. 2005/0188230 A1, published Aug. 25, 2005 (Ex. 1007).

Prelim. Resp. 6–15. The argument is based on a prior litigation in which a jury determined that Intel infringed the '373 patent ("the Intel litigation"). Ex. 1031 (March 2, 2021, verdict).

Patent Owner addresses each of the *Fintiv* factors for evaluating parallel litigation involving the challenged claims. *See* Prelim. Resp. 7–15. Petitioner submits that the factors have limited applicability here, because invalidity was not determined by the verdict. Prelim. Reply 3.

Because the Intel litigation is complete, there is no possibility of a stay. *See* Prelim. Resp. 11. Similarly, the Intel litigation has a known outcome and investment. *Id.* at 7–9 (discussing *Fintiv* factors 1, 2, and 3). On the other hand, invalidity was not presented to the jury, and Petitioner was not a party in the Intel litigation. *Id.* at 10–13.

In our view, Petitioner correctly emphasizes *Fintiv*'s language noting that the Board generally disfavors discretionary denial when litigation did not involve the petitioner, unless "the issues are the same as, or substantially similar to those already or about to be litigated, or other circumstances weigh against redoing the work of another tribunal." *Fintiv*, IPR2020-00019, Paper 11, 13–14. Indeed, in multiple decisions Patent Owner cites for support, the Board determined that instituting review would require resolving issues that would also have been resolved by a district court. *E.g.*, *Fitbit, Inc. v. Philips N. Am. LLC*, IPR2020-00828, Paper 13, 15–16 (considering the patent owner's litigation with a non-petitioning party that would overlap with the *inter partes* review at issue); *Mylan Labs. Ltd. v. Janssen Pharmaceutica N.V.*, IPR2020-00440, Paper 17, 19–23 (same, and additionally considering litigation involving the petitioner).

Here, because the Intel litigation did not resolve issues presented by this proceeding, there is no chance of an inconsistent outcome. Indeed,

"redoing the work of another tribunal" would only arise when that tribunal has resolved a dispute at issue before the Board. Patent Owner has not argued that resolving a dispute in this proceeding would conflict with an aspect of the Intel litigation. Thus, we do not agree with Patent Owner that, because "the [litigation] parties and the Court invested enormous amounts of time and money litigating validity and infringement issues relating to the '373 [patent]," instituting review here would mean redoing the work of another tribunal. Prelim. Resp. 12.

Patent Owner argues that instituting review here would lead to harassment of Patent Owners who prevail at trial, and that such an outcome fundamentally conflicts with Board precedent and policy. *Id.* at 15. We do not agree that prevailing in litigation against one party should insulate a patent owner from challenge by a different party based on grounds that were not resolved in the litigation.

Considering all of the *Fintiv* factors, we are persuaded that we should not exercise our discretion to deny institution in light of the Intel litigation.

2. Prior petitions

In IPR2020-00158, Intel challenged the '373 patent, and the Board denied institution. *Intel Corp. v. VLSI Technology LLC,* IPR2020-00158, Paper 16 (May 20, 2020) (the "Intel IPR"). Importantly, however, it did so based on parallel district-court litigation. *See* IPR2020-00158, Paper 16, 4–14. That denial did not consider the merits of Intel's challenge.

Patent Owner argues that we should exercise discretion to deny institution because the Petition presents the same challenges as the Intel IPR for which the Board denied review. Prelim. Resp. 16–25. In that regard, Patent Owner relies on the framework from *General Plastic Industrial Co.,*

Ltd. v. Canon Kabushiki Kaisha, IPR2016-01357, Paper 19 (Sept. 6, 2017) (precedential).

Factor 1: whether the same petitioner previously filed a petition directed to the same claims of the same patent

"[W]hen different petitioners challenge the same patent, we consider any relationship between those petitioners when weighing the *General Plastic* factors." *Valve Corp. v. Elec. Scripting Prods. Inc.*, IPR2019-00062, Paper 11, 9 (Apr. 2, 2019). In *Valve*, however, the petitioner and the prior petitioner were co-defendants accused of infringement based on the same product. *Id.* at 9–10. Patent Owner argues that the Board has found a relationship between petitioners when one uses substantive challenges from an earlier petition. Prelim. Resp. 21 (citing *Ericsson Inc. v. Uniloc 2017 LLC*, IPR2019-01550, Paper 8, 12). *Ericsson* imposed a relationship in light of the derivative nature of the petition at issue. *Ericsson*, IPR2019-01550, Paper 8, 12. That decision, however, has not been designated as precedential or informative by the Board, and other decisions have determined that factor 1 weighs against discretionary denial for an independent petitioner. *E.g.*, *United Fire Protection Corp. v. Engineered Corrosion Solutions, LLC*, IPR2018-00991, Paper 10 (determining that petitioner independence weighed against discretionary denial, but that substantive similarity with an unrelated prior petition meant the factor only moderately weighed against discretionary denial). We determine that factor 1 weighs somewhat against discretionary denial because Petitioner has not filed a prior petition, but did copy its substantive grounds from a prior petition.

That the Board has not substantively addressed the merits of the prior petitions, in our view, weighs against discretionary denial, because that approach best balances the desires to improve patent quality and patent-

system efficiency against the potential for abuse of the review process by repeated attacks on patents. *See General Plastic*, IPR2016-01357, Paper 19, 16–17. We view substantive consideration as an important factor in that balance, because to determine otherwise would asymmetrically insulate patent owners from potential abuse without addressing the desire to improve patent quality. Patent Owner suffers no abuse from having this tribunal consider the merits of these grounds for the first time.

Factor 2: whether at the time of filing of the first petition the petitioner knew of the prior art asserted in the second petition or should have known of it; and
Factor 4: the length of time that elapsed between the time the petitioner learned of the prior art asserted in the second petition and the filing of the second petition;
Factor 5: whether the petitioner provides adequate explanation for the time elapsed between the filings of multiple petitions directed to the same claims of the same patent;

Patent Owner argues that the public was on notice of the grounds asserted in the Intel IPR, and that PQA has thus not offered an adequate explanation of waiting to file the Petition here. Prelim. Resp. 19–20. PQA notes that it filed the Petition one month after PQA's formation. Prelim. Reply 6. We recognize that PQA was not formed until after the Intel litigation verdict, but agree with Patent Owner that PQA's members' knowledge before forming the entity is nonetheless relevant to our inquiry. *See* Prelim. Sur-Reply 5–6. Even presuming that PQA's members were aware of the Intel litigation or IPR, however, does not mean PQA's timing for the Petition is unexplained or unjustified.

Petitioner submits that institution is warranted because of changed circumstances—Intel's petition was denied in deference to district-court litigation, but that litigation concluded without deciding invalidity. Prelim.

Reply 5–6. At that time, Intel maintained invalidity grounds before the district court, justifying our exercise of discretion under *Fintiv* not to address those grounds. But Intel's decision to drop invalidity meant that no tribunal would consider those grounds. Patent Owner agrees that invalidity was dropped from the Intel litigation on "the eve of trial." Prelim. Resp. 5.

We determine that PQA has offered a reasonable explanation for the timing of the Petition, and conclude that factors 2, 4, and 5 weigh neither for nor against discretionary denial.

Factor 3: whether at the time of filing of the second petition the petitioner already received the patent owner's preliminary response to the first petition or received the Board's decision on whether to institute review in the first petition

Patent Owner argues that because Petitioner reviewed both Patent Owner's preliminary responses and also the Board's institution decisions from the Intel IPR, factor 3 strongly supports discretionary denial. Prelim. Resp. 23. Although Petitioner may have benefited from Patent Owner's preliminary response, Patent Owner has not identified how the institution decisions denying review based on *Fintiv* created any further imbalance. Those decisions did not discuss any substantive aspects of Intel's petitions, and did not allow Petitioner to modify its approach through roadmapping. *See* IPR2020-00106, Paper 17 (discussing only discretionary denial under *Fintiv*); IPR2020-00498, Paper 16 (same).

Petitioner's ability to review Patent Owner's preliminary response in the Intel IPR allowed Petitioner to address those arguments before filing the present Petition. Patent Owner provides a comparison between the Petition and Intel's petition in IPR2020-00158. Ex. 2016. That comparison shows some minor additions in the Petition, along with some omissions. *See, e.g.*,

id. at 22 (a statement regarding Harris's disclosures added to PQA's Petition), 25–26 (justification in Intel's petition omitted from PQA's Petition), 29 (summary of Harris's disclosures), 30 (summary of Harris's disclosures), 31 (addressing Harris's failure mode). None of those differences are material to our decision below that the Petition justifies institution, and we therefore conclude that Petitioner was not unfairly advantaged through roadmapping.

We conclude that factor 3 weighs in favor of discretionary denial.

Factor 6: the finite resources of the Board; and
Factor 7: the requirement under 35 U.S.C. § 316(a)(11) to issue a final determination not later than 1 year after the date on which the Director notices institution of review

Patent Owner submits that the Board has expended sufficient resources reviewing the Intel IPR, and that institution would "flood the Board with belated challenges to patents that have already been challenged and/or litigated." Prelim. Resp. 24; *accord* Prelim. Sur-Reply 6. That assertion, however, fails to distinguish between the Board expending resources on substantive consideration (which it has not done for the '373 patent) and considering why another forum may be better suited to do so (as in the Intel IPR). Without any Board proceeding requiring ongoing resources for the '373 patent, we conclude that factors 6 and 7 weigh against discretionary denial.

Summary

Having considered all the *General Plastic* factors, based on the present record, we conclude that most factors support institution whereas only one factor weighs against institution. We therefore determine not to exercise our discretion to deny institution under § 314(a).

3. Previously presented arguments and consistent exercise of discretion

Patent Owner argues we should deny the Petition because it is a substantive copy of the Intel IPR petition. Prelim. Resp. 25–27. In Patent Owner's view, the Federal Circuit's recent *Vivint* case directs such a result. *Id.* at 25 (citing *In re Vivint, Inc.*, 14 F.4th 1342 (Fed. Cir. 2021)). Patent Owner argues that we should deny institution under § 325(d) because *Vivint* "confirms that denial under § 325(d) is required here." Prelim. Resp. 26. We do not agree.

The Federal Circuit held that "the Patent Office, when applying § 325(d), cannot deny institution of IPR based on abusive filing practices then grant a nearly identical reexamination request that is even more abusive." *Vivint*, 14 F.4th at 1354. It found important that, when the Board denied Alarm.com's IPR petition, the Board considered Alarm.com's earlier petitions and reasoned that "allowing similar, serial challenges to the same patent, by the same petitioner, risks harassment of patent owners and frustration of Congress's intent in enacting the [AIA]." *Id.* at 1353 (quoting IPR2016-01091, Paper 11, 12) (alteration in original) (emphasis omitted).

The facts here are not remotely similar. The Intel IPR was not denied for abusive filing practices, but rather was denied to avoid overlap with a parallel district-court litigation. *See* IPR2020-00158, Paper 16, 4–14. This proceeding involves a different petitioner, which has not before petitioned for review of the '373 patent. Those facts show that this Decision does not involve potentially abusive filing practices by the same challenger, as was at issue in *Vivint*.

Patent Owner has not identified how instituting review would be inconsistent with a prior decision on this patent. As explained above, because no invalidity issue was presented in district court underlying the

prior application of *Fintiv*, we reach a different conclusion under that doctrine based on different facts here. Thus, *Vivint* is not germane to our decision.

As to the merits of Patent Owner's position that we should decline institution under § 325(d), that argument is not persuasive. The arguments in the Petition were previously presented to the office, in the Intel IPR. *See Advanced Bionics, LLC v. MED-EL Elektromedizinische*, IPR2019-01469, Paper 6, 8 (PTAB Feb. 13, 2020) (precedential). Thus, we consider factors including the Office's record from prior reviews and Petitioner's showing of error in that consideration. *Id.* at 10. Our evaluation of Petitioner's substantive challenge persuades us that the Petition presents a sufficient basis to proceed with institution here. We therefore do not discretionarily deny review in light of the Intel IPR petition.

B. UNPATENTABILITY OVER HARRIS, ABADEER, AND ZHANG

Petitioner submits that claim 1 would have been obvious over Harris, Abadeer, and Zhang. Petitioner relies on Harris for a system including switchable voltages provided to memory and other system in an integrated circuit.

Harris discloses a system for permitting "soft defect detection testing (SDDT)" of a memory array in a data processor. Ex. 1003, code (57). Harris's Figure 1 is reproduced below:

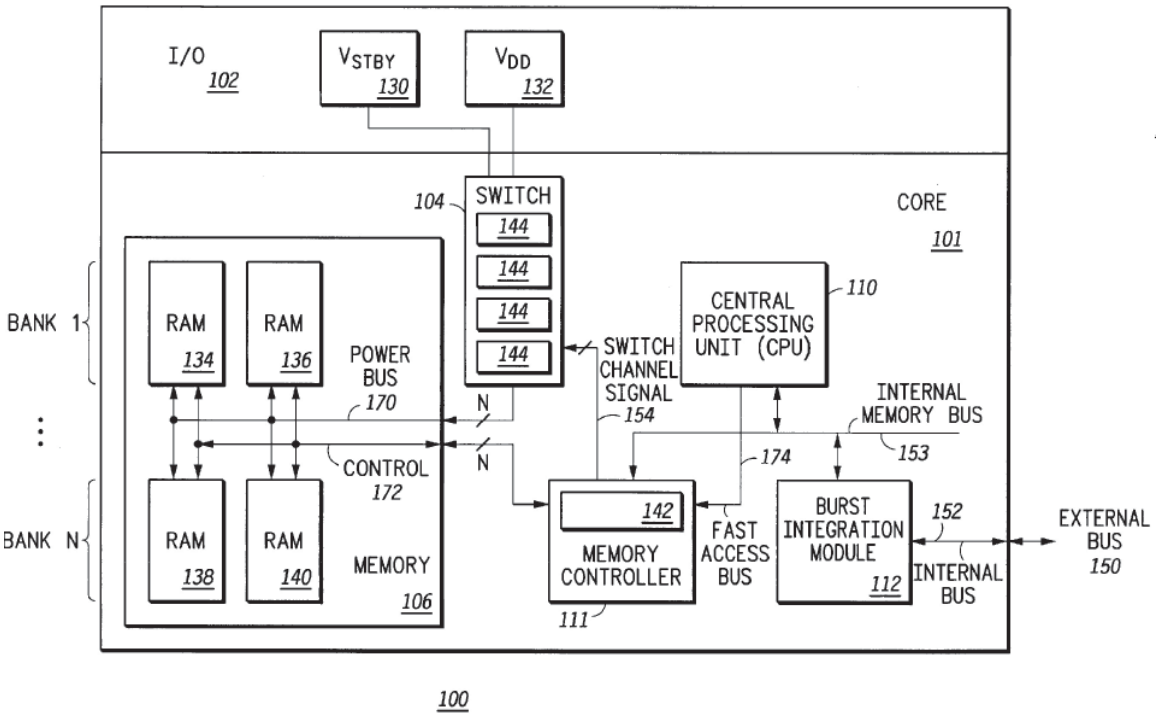

FIG.1

Id., Fig. 1. Figure 1 depicts data processor 100 with core 101 including memory portion 106 and switch circuit 104 with a plurality of switches 144 that couple two power-supply terminals in I/O section 102, Vstby 130 and VDD 132, to power bus 170 providing power to memory portion 106. *Id.* 2:27–67.

Harris states that, "[i]n a normal mode of operation, the core 101 would be powered by a supply voltage applied to VDD terminal 132." *Id.* at 3:1–2. It then describes the SDDT operation, in which CPU 110 writes to register 142 in memory controller 111, causing switch 104 to power a portion of memory 106 from the Vstby terminal rather than the VDD terminal. *Id.* at 3:10–36. When so powered, an external circuit that applies power to the Vstby terminal may measure the current drawn by the portion of memory powered by Vstby, detecting whether that portion has a defect. *Id.* at 3:36–49.

Harris describes that "the Vstby pin has a hardware controlled function as well," which is "the normal standby voltage function of the Vstby pin." *Id.* at 3:50–54. For that function, "the voltage level on the terminal VDD 132 is monitored to ensure that a functional voltage is provided." *Id.* at 3:54–56. "When this VDD voltage level drops below a set level or threshold, the voltage on the Vstby terminal 132 is switched to power the memory 106 to sustain memory contents when either main or VDD power is failing." *Id.* at 3:57–60. Thus, in the failure mode, the memory contents are preserved by switching the memory to a power supply of sufficient voltage when the main supply drops below that level.

Harris further describes a low-power feature:

> [T]he test mode of the data processor data processor taught herein may be used as a low power feature wherein the second power supply voltage (Vstby or Vdd) is provided to the at least one memory array while the first power supply voltage (Vdd or Vstby) which is being supplied to the CPU is lowered so that lower power is consumed in the data processor while data within the at least one memory array is maintained.

Id. at 4:64–5:4.

Petitioner asserts that Abadeer discloses determining a memory's minimum operating voltage and storing that voltage's value in nonvolatile memory. Pet. 15–19, 27–30. Abadeer discloses "[a] solution for determining minimum operating voltages due to performance/power requirements." Ex. 1004, code (57). It states that its method applies to determining a minimum operating voltage for a "voltage island," in an integrated circuit, such as a memory array. *Id.* ¶ 12. By that, Abadeer aims to reduce power consumption in semiconductor circuits. *Id.* ¶ 13. Once a minimum operating voltage is determined in Abadeer, it is stored in nonvolatile memory. *Id.* ¶¶ 44–45.

Petitioner submits that skilled artisans had reason to use those teachings from Abadeer with Harris's system because (1) Harris teaches memory loss may occur below a threshold voltage, but accommodates known approaches in determining the threshold, such as Abadeer's; (2) both Harris and Abadeer refer to reducing power consumption while maintaining a threshold voltage for memory; (3) Harris's and Abadeer's teachings are compatible and Abadeer's technique would have predictably applied to Harris's system. *Id.* at 30–33.

Petitioner asserts that Zhang discloses voltage regulators applicable to Harris's system. Pet. 19–21, 36. Zhang discloses a system including "one or more integrated voltage regulators powered by an external voltage regulator and generating one or more local supply voltages for the processor." Ex. 1005, code (57); *see also id.* ¶¶ 18–31.

Petitioner submits that skilled artisans had reason to use Zhang's voltage regulators to supply the voltages for Harris's circuit. Pet. 35–40. Specifically, Petitioner asserts that skilled artisans had reason to use Zhang's regulators (1) to provide stable, precise supply voltages, facilitating accurate testing with Harris's test mode; (2) to decrease power consumption by making voltages adjustable; and (3) because doing so would have predictably added Zhang's benefits to Harris's system. *Id.* at 37–39.

As to claim 1's requirement of providing different voltages to the memory circuit depending on the levels of the two voltages in the claimed circuit, Petitioner relies on both Harris's "low power feature" and also its failure mode. Pet. 44–46.

1. Harris's low-power feature

Patent Owner argues that Harris's low-power feature does not switch the memory between voltages and instead "provide[s] the memory with an independently adjusted voltage using one voltage plane, while providing other circuity with another independently adjusted voltage using the other voltage plane." Prelim. Resp. 34. The distinction is whether the voltage provided to the memory is itself adjusted to accommodate the memory's needs, or instead whether the memory is provided with power from a different voltage source to change the memory's voltage. Prelim. Resp. 36–40.

Patent Owner's distinction is not consistent with Harris's disclosures. Harris describes that a switch determines whether a particular memory block is provided with VDD or Vstby. Ex. 1003, 3:15–16. While that disclosure is made in the context of Harris's "soft defect detection test (SDDT)" functionality, Harris states that "the test mode of the data processor . . . may be used as a low power feature," instructing that the same hardware may operate to provide other functions such as the low-power feature. *Id.* at 4:64–65.

Patent Owner argues that Harris's low-power feature does not disclose switching the memory from one power supply to another, and does not disclose including a switch at all when implementing the low-power feature. Prelim. Resp. 36–37. We do not agree. Harris describes that "[i]n a normal mode of operation, the core 101 would be powered by a supply voltage applied to the VDD terminal 132." Ex. 1003, 3:1–2. Nothing about that description limits it to a particular implementation, and because Harris's memory is part of its core (*id.* at 2:33–34), Harris discloses that memory is powered by VDD in normal operation. When describing the low-power

feature, Harris describes that "the second power supply voltage (Vstby or Vdd) is provided to the at least one memory array while the first power supply voltage (Vdd or Vstby) which is being supplied to the CPU is lowered . . . ." *Id.* at 4:66–5:2. Thus, Harris discloses selecting between the two available power supplies to provide power to the memory. That selecting (with Harris's switch 104) is consistent with Patent Owner's understanding that "Harris's processor contains two separate voltage planes, Vstby and VDD." *See* Prelim. Resp. 32. Thus, on the present record, we conclude that Harris's low-power feature discloses the claimed switching.

2. Harris's failure mode

Patent Owner addresses Harris's failure mode separately from Harris's low-power feature. *See* Prelim. Resp. 40–44. In Patent Owner's view, the claims cannot read on Harris's failure mode because that mode describes switching the memory to the standby supply only "when either main or VDD power is failing." *Id.* at 41 (quoting Ex. 1003, 3:59–60). Patent Owner points out that claim 1 requires providing a regulated voltage to the functional circuit (i.e., non-memory) when switching the memory to a separate power supply. *Id.* at 41–42. Patent Owner submits that Harris's failure mode would not satisfy that limitation because "[a] failed voltage is not a regulated voltage." *Id.* at 41. Patent Owner argues also that, even if one were to consider a failed voltage to be "regulated" as required by the claims, a skilled artisan would not continue supplying a failing voltage to the non-memory portions of the circuit. *Id.* at 41–42.

When Harris describes a condition where "VDD power is failing," it is possible such a VDD supply no longer provides a "regulated voltage" as required by the claim. The present record does not, however, compel such a

determination and we conclude that it is best to resolve the dispute at trial. We need not resolve that dispute at this time, as we conclude that Harris's low-power feature justifies institution. Because the instituted trial includes all asserted grounds, the parties may further develop the record regarding whether and, if so, when a failing power supply no longer provides a regulated voltage as required by the claims.

3. Zhang's voltage regulators

Patent Owner also disputes whether skilled artisans had reason to use Zhang's voltage regulators with Harris's selectable voltage supplies. Prelim. Resp. 38–40. In Patent Owner's view, because Zhang teaches independently adjustable voltage regulators, it would not make sense to use those in a system that switches between power supplies to change the voltage provided to a particular component. *Id.* Patent Owner reasons that "Zhang has no need for such functionality." *Id.* at 38. Whether Zhang has a need is not at issue, however, because Petitioner asserts a combination in which Zhang's regulators are used in Harris's system. *See* Pet. 36–40.

Patent Owner submits that there would be no reason to switch the memory between power supplies if each is independently controlled. Prelim. Resp. 39. As discussed above, we do not agree that Harris's low-power feature lacks switching between power supplies. Thus, we do not agree with Patent Owner that Petitioner needs to justify a system that switches its memory between power supplies. The present record supports that Harris already operates in that manner.

Patent Owner submits that, when considering the two references together, a skilled artisan would use Zhang's voltage regulators to implement a "switchless approach" to providing various voltage levels to

different components. Prelim. Resp. 40. We determine that the present record adequately supports Petitioner's contentions regarding the asserted combination, and that Patent Owner's argument establishes at most a factual dispute that is best resolved at trial. The parties may further address this dispute at trial.

4. Relative voltages

As to whether the voltage provided to the memory is greater than the voltage provided to the functional circuit, Patent Owner relies on its expert to argue that "Harris does not teach that VDD would fall below Vstby." Prelim. Resp. 48 (quoting Ex. 2002 ¶ 100). But that contention is not consistent with Harris's disclosures. Harris states that, in the low-power feature, one of the two voltages is provided to the memory while the other is provided to the CPU, and the voltage "supplied to the CPU is lowered so that lower power is consumed in the data processor while data within the at least one memory array is maintained." Ex. 1003, 4:66–5:4. By keying the feature to maintaining memory data while lowering CPU voltage, Harris discloses that the CPU voltage is less than the memory voltage.

5. Combining embodiments

Patent Owner argues that "Harris teaches three distinct embodiments" in its SDDT, power-failure, and low-power disclosures. Prelim. Resp. 52–55. That view misconstrues Harris. Harris is clear that those three disclosures largely relate to the same underlying hardware. It first describes the hardware used to implement SDDT. Ex. 1003, 3:3–49. In SDDT, Harris explains that the CPU writes to register 142 to indicate to switch 104 that test mode is entered, causing the switch to power at least a portion of memory 106 with Vstby instead of VDD. *Id.* at 3:10–29. Then, Harris

explains that "the Vstby pin has a hardware controlled function as well," which is "the normal standby voltage function of the Vstby pin. *Id.* at 3:52–54. That function uses the same switching hardware as in SDDT to power memory from Vstby when "VDD voltage level drops below a set level or threshold," thus "sustain[ing] memory contents when either main or VDD power is failing." *Id.* at 3:57–60. Harris explains that "the present invention allows for dual functionality of the voltage standby (Vstby) pin" and summarizes:

> One function being a VDD failure mode where a failure is detected on the VDD pin 132 and Vstby must be substituted for VDD to avoid memory data loss, and the other mode being software controlled mode which allows for the testing of soft defects using an external SDDT current measurement which is improved over the prior art.

Id. at 3:63–4:3. Harris presents the "low power feature" in a similar way, stating that "the test mode of the data processor . . . taught herein may be used as a low power feature." *Id.* at 4:64–65. Because Harris's explanations of the three operating modes (SDDT, power failure, and low power) all arise from and relate to the same underlying hardware system, we do not agree with Patent Owner that Petitioner needs to justify reliance on Harris's multiple operating modes.

6. Compatibility between Harris and Zhang

Patent Owner argues that Petitioner fails to present a cohesive challenge, in that it relies on Zhang's voltage regulators to provide a stable voltage, but relies on Harris's VDD failing and lacks proof "that Harris's now-regulated VDD would continue to fail under [Petitioner's] proffered modification." Prelim. Resp. 56–58. We do not agree that Petitioner applies the art inconsistently.

For example, Patent Owner asserts that Petitioner "relies ***exclusively*** upon VDD failing" for limitation 1[h]. *Id.* at 56 (citing Pet. 43–44). We read the Petition differently. Limitation 1[h] recites "providing the first regulated voltage as the operating voltage of the memory when the first regulated voltage is at least the value of the minimum operating voltage." Petitioner relies on a portion of Harris's described failure behavior to support that the first voltage (VDD) is provided to all parts of the circuit, including the memory, when VDD is above a certain voltage threshold. Pet. 43–44 (citing Ex. 1003, 3:1–2, 3:53–4:3; Ex. 1002 ¶ 94–96). Petitioner's assertions address behavior of the underlying hardware system, and do not conflict with how the system is used in various circumstances. Stated otherwise, we do not agree that Petitioner relies on Harris's failure mode itself for limitation 1[h]. Rather, Petitioner relies on aspects of Harris's description that a skilled artisan would understand to apply also in Harris's low-power feature.

As to compatibility with Zhang, we determine that Petitioner relies on aspects beyond Harris's failure-mode operation, such as the low-power feature discussed above. Thus, any potential incompatibility between including Zhang's voltage regulators and Harris's failure-mode operation would not affect our decision to institute.

Additionally, we do not read the record to support that adding Zhang's voltage regulators to Harris's circuit would itself address a power-supply failure. Patent Owner identifies evidence regarding the normal operation of Zhang's voltage regulators. *See* Prelim. Resp. 56–58. Patent Owner has not identified evidence addressing how Zhang's voltage regulators respond to a failing voltage supply. *Id.* We do not agree that we should conclude, on the present record, that Zhang's voltage regulators would overcome a failing

power supply. Rather, Zhang suggests that without a functioning supply voltage, a regulator would be unable to operate. *See* Ex. 1005 ¶ 35 (describing that "[s]upply voltage 355 is provided to power the circuit" for Zhang's voltage regulator in Fig. 3B). Thus, we conclude that Zhang's voltage regulators would not eliminate the possibility of a failing power supply. Accordingly, a combination of Zhang's voltage regulators with Harris's circuit is not inherently inconsistent.

7. Objective evidence of nonobviousness

Patent Owner submits that a jury's large damages award against Intel shows that the invention claimed in the '373 patent is commercially successful. Prelim. Resp. 59. Patent Owner further asserts that the damages award was expressly connected to the value of the patented aspects apart from any unpatented features. *Id.* at 60.

Petitioner has not yet had an opportunity to respond to Patent Owner's arguments regarding objective indicia of nonobviousness. Patent Owner's arguments will ultimately depend on resolving potential factual disputes and balancing competing factors. We determine those arguments are best suited for resolution through trial.

8. Summary

Other than as discussed above, Patent Owner does not challenge Petitioner's contentions for unpatentability over Harris, Abadeer, and Zhang. Based on the present record, we conclude that Petitioner has shown a reasonable likelihood it will prevail with respect to unpatentability of claim 1 over Harris, Abadeer, and Zhang—Petitioner's showing justifies institution. Pet. 25–46. Our conclusion considers Petitioner's stated motivations for modifying Harris in light of Abadeer and Zhang.

We have reviewed Petitioner's contentions for claims 2–7, 9–11, and 13–16 as unpatentable over Harris, Abadeer, and Zhang (Pet. 47–67), and reach the same conclusions for those claims.

C. Unpatentability Grounds including Cornwell or Bilak

Patent Owner does not separately challenge Petitioner's grounds that include Cornwell or Bilak with Harris, Abadeer, and Zhang. We have reviewed Petitioner's contentions for (1) claims 2, 11, and 12 as unpatentable over Harris, Abadeer, Zhang, and Cornwell (Pet. 67–72); and (2) claim 8 as unpatentable over Harris, Abadeer, Zhang, and Bilak (Pet. 72–74) and conclude that Petitioner has shown a reasonable likelihood it will prevail with respect to those grounds.

III. CONCLUSION

For the reasons discussed above, we conclude Petitioner has shown a reasonable likelihood of prevailing with respect to at least one claim. We have evaluated all of the parties' submissions and determine that the record supports institution. We conclude that instituting review in this proceeding is in the interest of efficient administration of the Office and the integrity of the patent system. *See* 35 U.S.C. § 316(b). Accordingly, we institute an *inter partes* review of all challenged claims under all grounds set forth in the Petition.

Our determination at this stage of the proceeding is based on the evidentiary record currently before us. This decision to institute trial is not a final decision as to patentability of any claim for which *inter partes* review has been instituted. Our final decision will be based on the full record developed during trial.

IV. ORDER

Accordingly, it is

ORDERED that, pursuant to 35 U.S.C. § 314(a), *inter partes* review of the '373 patent is instituted on the claims and grounds set forth in the Petition;

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial commencing on the entry date of this decision.

PETITIONER:

Bruce Slayden
Truman Fenton
Tecuan Flores
SLAYDEN GRUBERT BEARD PLLC
bslayden@sgbfirm.com
tfenton@sgbfirm.com
tflores@sgbfirm.com

PATENT OWNER:

Baback Redjaian
IRELL & MANELLA LLP
bredjaian@irell.com

Kenneth J. Weatherwax
Bridget Smith
Flavio Rose
Edward Hsieh
Parham Hendifar
Patrick Maloney
Jason C. Linger
LOWENSTEIN & WEATHERWAX LLP
weatherwax@lowensteinweatherwax.com
smith@lowensteinweatherwax.com
rose@lowensteinweatherwax.com
hsieh@lowensteinweatherwax.com
hendifar@lowensteinweatherwax.com
maloney@lowensteinweatherwax.com
linger@lowensteinweatherwax.com